What Is Claimed Is:

1. An amplifier circuit, comprising:
an operational amplifier having a non-converting input terminal coupled to a ground, a converting input terminal, and an output terminal; and
a resistor network comprising a plurality of stages connected serially, coupled between the converting input terminal and the output terminal, wherein each stage of the resistor network comprises:
an input node;
an output node;
a first resistor coupled between the input node and the ground; and
a second resistor coupled between the input node and the output node.

2. The amplifier circuit as claimed in claim 1, wherein the resistance of the first resistor is two times larger than the resistance of the second resistor.

3. The amplifier circuit as claimed in claim 2, wherein the equivalent resistance of the resistor network is $2^n \times R$, wherein the resistor network includes n stages and the resistance of the second resistor is R.

4. An amplifier circuit, comprising:
an operational amplifier having a non-converting input terminal coupled to a ground, a converting input terminal, and an output terminal;

a first resistor network comprising a plurality of stages connected serially, coupled to the converting input terminal for receiving an input voltage, wherein each stage of the first resistor network comprises:

an input node;

an output node;

a first resistor coupled between the input node and the ground; and

a second resistor coupled between the input node and the output node; and

a loading unit coupled between the converting input terminal and the output terminal.

5. The amplifier circuit as claimed in claim 4, wherein the resistance of the first resistor is two times larger than the resistance of the second resistor.

6. The amplifier circuit as claimed in claim 5, wherein the equivalent resistance of the resistor network is $2^n \times R$, wherein the resistor network includes n stages and the resistance of the second resistor is R.

7. The amplifier circuit as claimed in claim 4, wherein the loading unit is a second resistor network comprising a plurality of stages connected serially, wherein each stage of the first resistor network comprises an input node, an output node, a third resistor coupled between the input node and the ground, and a fourth resistor coupled between the input node and the output node.

8. The amplifier circuit as claimed in claim 7, wherein the resistance of the third resistor is two times larger than the resistance of the fourth resistor.

9. The amplifier circuit as claimed in claim 8, wherein the equivalent resistance of the resistor network is $2^n \times R$, wherein the resistor network includes n stages and the resistance of the fourth resistor is R.

10. A resistor network includes a plurality of stages connected serially, wherein each stage of the first resistor network comprises:

an input node;

an output node;

a first resistor coupled between the input node and the ground; and

a second resistor coupled between the input node and the output node, wherein the resistor network is implemented inside of an IC device.

11. The amplifier circuit as claimed in claim 10, wherein the resistance of the first resistor is two times larger than the resistance of the second resistor.

12. The amplifier circuit as claimed in claim 11, wherein the equivalent resistance of the resistor network is $2^n \times R$, wherein the resistor network includes n stages and the resistance of the second resistor is R.

13. The amplifier circuit as claimed in claim 10, wherein each of the first resistor and the second resistor is implemented by a MOS transistor.